CLAIMS

Please amend claims as shown in the following claim listing.

1-67. (Canceled).

68. (Currently Amended) A method comprising:

identifying by an operating system entry of a processor into a C power state ~~of an~~ in accordance with Advanced Configuration and Power Interface ~~specification~~ (ACPI) Specification, Revision 2;

reading by the operating system a time corresponding to an exit of the processor from the C power state, wherein the processor exits from the C power state in response to an interrupt, wherein the processor executes an interrupt routine in response to the interrupt, and wherein the time corresponding to the exit is identified in response to the interrupt and prior to execution of the interrupt routine; and

determining by the operating system a duration corresponding to the C power state based on the time corresponding to the exit.

69. (Previously Presented) The method of claim 68, wherein the C power state is a C1 power state.

70. (Previously Presented) The method of claim 68, wherein the C power state is entered in response to a halt instruction.

71. (Previously Presented) The method of claim 68, comprising:

causing by the operating system the time corresponding to the exit to be identified in response to the interrupt and prior to execution of the interrupt routine.

72. (Previously Presented) The method of claim 68, comprising storing by the operating system the time corresponding to the exit in main memory.

73. (Previously Presented) The method of claim 68, comprising storing by the operating system the time corresponding to the exit in the processor.

74. (Previously Presented) The method of claim 68, comprising storing by the operating system the time corresponding to the exit in a chip.

75. (Previously Presented) The method of claim 68, comprising storing by the operating system the time corresponding to the exit in a chipset.

76. (Previously Presented) The method of claim 68, comprising identifying by the operating system a time corresponding to an entry of the processor into the C power state.

77. (Previously Presented) The method of claim 76, comprising storing by the operating system the time corresponding to the entry in main memory.

78. (Previously Presented) The method of claim 76, comprising storing by the operating system the time corresponding to the entry in the processor.

79. (Previously Presented) The method of claim 76, comprising storing by the operating system the time corresponding to the entry in a chip.

80. (Previously Presented) The method of claim 76, comprising storing by the operating system the time corresponding to the entry in a chipset.

81. (Previously Presented) The method of claim 68, wherein the reading includes reading a counter.

82. (Previously Presented) The method of claim 68, wherein the reading includes reading a counter in a chip.

83. (Previously Presented) The method of claim 68, wherein the reading includes reading a counter in a chipset.

84. (Previously Presented) The method of claim 68, comprising:

causing by the operating system a counter to be started in response to the identifying.

85. (Previously Presented) The method of claim 68, comprising:

causing by the operating system a counter to be halted in response to the interrupt.

86. (Currently Amended) The method of claim 68, comprising:

selecting by the operating system a C power state for the processor based on the determined duration; and

causing by the operating system the processor to enter the selected C power state.

87. (Currently Amended) A method comprising:

identifying by an operating system entry of a processor into a C power state ~~of an~~ in accordance with Advanced Configuration and Power Interface ~~specification~~ (ACPI) Specification, Revision 2;

causing by the operating system a counter to be started;

identifying by the operating system an exit of the processor from the C power state in response to an interrupt;

causing by the operating system the counter to be halted; and

determining by the operating system a duration corresponding to the C power state based on a content of the counter.

88. (Previously Presented) The method of claim 87, wherein the C power state is a C1 power state.

89. (Previously Presented) The method of claim 87, wherein the C power state is entered in response to a halt instruction.

90. (Previously Presented) The method of claim 87, wherein the processor executes an interrupt routine in response to the interrupt, and wherein the causing the counter to be halted is performed prior to execution of the interrupt routine.

91. (Previously Presented) The method of claim 87, wherein the counter is in a chip.

92. (Previously Presented) The method of claim 87, wherein the counter is in a chipset.

93. (Currently Amended) The method of claim 87, comprising:

selecting by the operating system a C power state for the processor based on the determined duration; and

causing by the operating system the processor to enter the selected C power state.